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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,748	07/15/2003	Nobuyuki Ishige	501.42822X00	6927

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EXAMINER	
DI GRAZIO, JEANNE A	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,748	ISHIGE ET AL.	
	Examiner	Art Unit	
	Jeanne A. Di Grazio	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-12* is/are pending in the application.

4a) Of the above claim(s) *4-7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 8-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/7/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims

Claims 1-2, and 8-12 are pending per Amendment and Response of October 7, 2005. Claims 4-7 have previously been withdrawn. Claims 10-12 are newly added claims per Amendment of October 7, 2005.

Priority

Priority to Japanese Patent Application No. 2002-207691 (July 17, 2002) is claimed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3 and 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 5,949,502 (to Matsunaga et al.) in view of United States Patent 5,914,763 (to Fujii et al.) and further in view of United States Patent 6,633,359 B1 (to Zhang et al.).

As to claims 1 and 10-12, Matsunaga teaches and discloses that a conventional liquid crystal display device has two transparent insulating substrates that enclose a layer of liquid crystal material (Column 1, Lines 12-16)(Applicant's "a liquid crystal layer between a first substrate and a second substrate"), a plurality of gate lines and drain lines that define pixel regions in which switching elements and transparent pixel electrodes are formed (Id. at Lines 16-

24)(Applicant's "the first substrate including a pixel area having pixel electrodes and a peripheral area surrounding the pixel electrodes, the pixel area including gate lines and drain lines, ..."), individual drain line groups and individual gate line groups extend into the periphery of the transparent insulating substrate to constitute external terminals which are connected with video drive circuits and gate scanning circuits (Id. at Lines 28-37)(Applicant's "the gate lines including first gate lines and second gate lines, first gate connecting lines and second gate connecting lines being disposed in the peripheral area, the respective first gate connecting lines electrically connecting the first gate lines to a liquid crystal driving circuit, the respective second gate lines electrically connecting the second gate lines to the liquid crystal driving circuit").

Matsunaga does not appear to explicitly specify that the first gate connecting lines and the second gate connecting lines are stacked in a thickness direction of the first substrate.

Fujii teaches and discloses a liquid crystal display with substantially equal resistances for sets of terminal electrodes and inclined wiring electrodes (Title, entire patent). Fujii teaches that connection electrodes and leadout wirings are arranged on sides of two substrates in a liquid crystal display device (Columns 6 and 7). Thereafter, the two substrates each bearing the connection electrodes and leadout wirings are stacked together at which point the connection electrodes and leadout wirings are mutually stacked with respect to each other (See, e.g., Column 14, Lines 12-46). Such a configuration allows for an equal gap at both the terminal section and the display section so that color variation is prevented (Id. Lines 43-46). This ultimately improves upon display quality (Id.).

Fujii is evidence that ordinary workers in the field of liquid crystal would have found the reason, suggestion and motivation to stack connection electrodes in a liquid crystal display device for uniform gap in both terminal and display sections so that color variation is prevented.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Matsunaga in view of Fujii for uniform gap in both terminal and display sections so that color variation is prevented and thus improved display quality.

Matsunaga does not appear to explicitly specify the stacking of first and second gate connecting lines or first and second insulating layer relationship as presently claimed.

Zhang generally discloses a liquid crystal display wherein first and second signal lines are stacked with first and second insulating films (Column 2, Lines 20-40). The signal lines are furthermore adjacent each other in a plan view.

It would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Matsunaga in view of Zhang for a low power consumption display (Zhang, Id.).

Thus, claims 1 and 10-12 are rejected.

As to claim 2, once the transparent substrates each bearing the connection electrodes and leadout electrodes are stacked, the various electrodes will be placed at different levels relative to each other (Fujii).

Thus, claim 2 is rejected.

As to claim 3, as noted, the pixel has a periphery and display area (Matsunaga).

Thus, claim 3 is rejected.

As to claim 8, as noted in regard to claim 2, once the substrates are overlapped the various electrodes will overlap in a plan view (Fujii).

Thus, claim 8 is rejected.

As to claim 9, both Matsunaga and Fujii teach and disclose various relationships among electrodes.

Thus, claim 9 is rejected.

Response to Arguments

Applicant's arguments with respect to said claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (571)272-2289. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeanne Andrea Di Grazio
Patent Examiner
Art Unit 2871

JDG

ANDREW SCHECHTER
PRIMARY EXAMINER